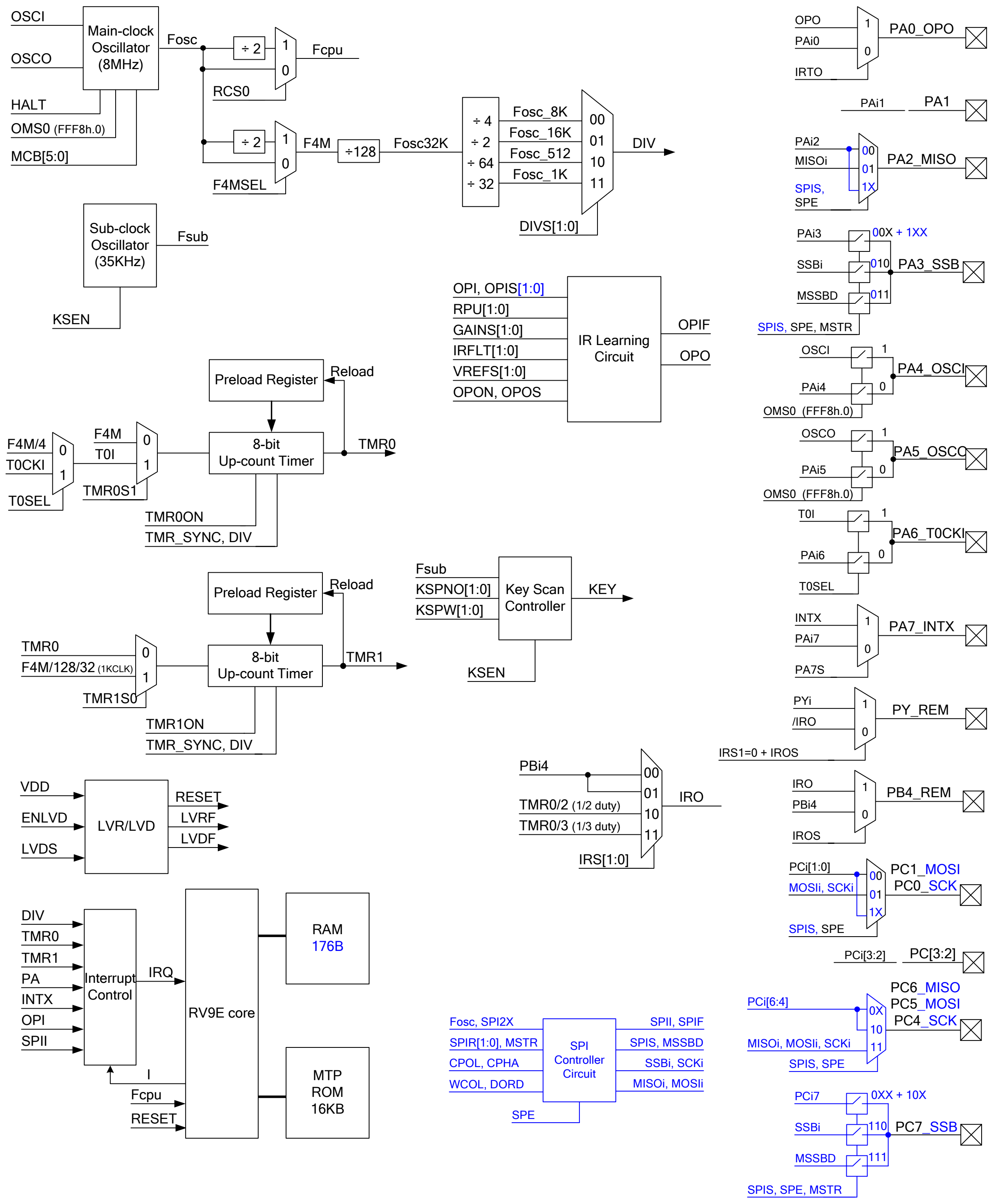
Revision History:

Date	Revision#	Description	Page
2013/06/24	005	1. Revise some errors	18
2013/06/19	004	1. Revise device name to ET56M017	4,10
		2. Revise 16 SOP package pin out	4
2013/06/13	003	1. Revise 14 SOP package pin out	4
		2. Revise some errors	17
2013/03/05	002	1. Change RAM size to 176B	2,3,5
		2. Add PA1PHS register bit to select PA1 pull-high R=10K or 300K	7,9,22
		3. Add a register bit to select IR learning edge detect interrupt mode	3,7,9,16
		4. Add SPIS register bit to select SPI interface pins	2~4,7,9,17,18
		5. Swap PC[1:0] SPI pin function	2~4,9
		6. Redefine SPIR[1:0] SCK clock rate	18
		7. Add a new 16 SOP package form	4
2012/12/25	001	New create	

Features

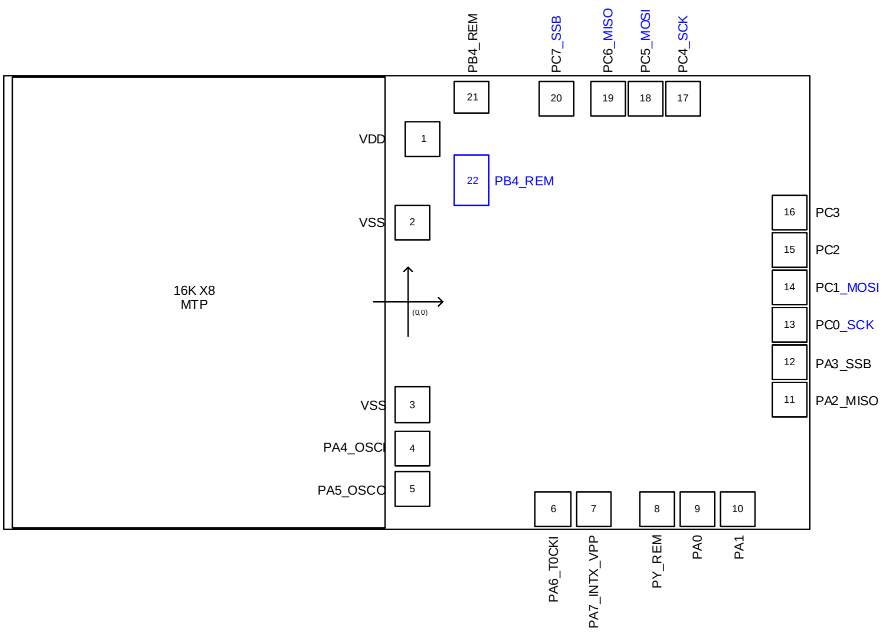
1. Operate voltage:
   - *1.8V~3.6V @ 8MHz*
2. Built-in Main-clock oscillator
   - *BR8M: Built-in RC 8MHz oscillator with 6 calibration bits (+/- 1%)*
   - *XT8M: External crystal 8MHz (No built-in C)*
3. 2 kinds of CPU speed: Fcpu=Fosc/1, Fosc/2
4. 2 kinds of CPU operating mode: Normal or Sleep.
5. RV9E CPU core
6. 16K bytes Program MTP ROM
7. 176 bytes General Purpose SRAM
8. 2 timers
   - *Timer 0: 8-bit timer*
   - *Timer 1: 8-bit timer*
9. 18 I/O pins:
   - *PA0(OPO)*, PA1, PA2(MISO)*, PA3(SSB)*, PA4(OSCI)*, PA5(OSCO)*, PA6(T0CKI)*, PA7(INTX(VPP))**
   - *PB4(REM)*, PY(REM)**
   - *PC0(SCK)*, PC1(MOSI)*, PC[3:2], PC4(SCK)*, PC5(MOSI)*, PC6(MISO)*, PC7(SSB)** **: share pin*
10. 7 interrupt sources:
    - *Divide interrupt time-base*
    - *Timer 0 interrupt*
    - *Timer 1 interrupt*
    - *PA interrupt: When the falling edge transition in port A*
    - *External interrupt*
    - *IR learning input interrupt*
    - *SPI interrupt*
11. Built-in IR learning function
12. Key scan wake up function
13. SPI function
14. LVR/LVD function
15. COB or 14/16/20 SOP package form

Block Diagram



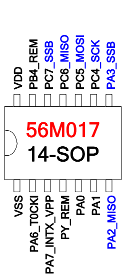
Pad Description

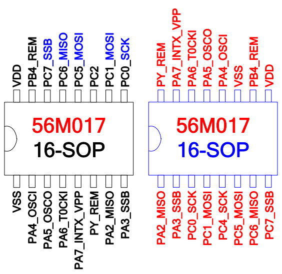
No.	Name	I/O	Description
	PC7_SSB, PC6_MISO, PC5_MOSI, PC4_SCK, PC3 PC2,PC1_MOSI, PC0_SCK	I/O	Bi-directional 8-bit I/O port. It can be configured as CMOS output or input. PC7_SSB, PC6_MISO, PC5_MOSI, PC4_SCK, PC1_MOSI and PC0_SCK also shared with SPI pins.
	PB4_REM	O	1-bit O/P port. It can be configured as CMOS or NMOS output. PB4_REM also shared with IR output function.
	PY_REM	I/O	Bi-directional 1-bit I/O port. It can be configured as CMOS output or input with or without pull-high resistor. PY_REM also shared with IR output.
	VDD, VSS, VSS	P	Power supply
	PA6_T0CKI, PA5_OSCO, PA4_OSCI, PA3_SSB, PA2_MISO, PA1, PA0	I/O	7-bit I/O port. It can be configured as output port (CMOS or NMOS output) or input port (with or without pull-high resistors). PA6_T0CKI also shared with external clock T0CKI input function. PA5_OSCO & PA4_OSCI also shared with main oscillator clock pins. PA3_SSB and PA2_MISO also shared with SPI chip select and data I/O pins.
	PA7_INTX_VPP	I	1-bit input port. It can be configured as input with or without pull-high resistors. PA7_INTX_VPP also shared with external interrupt and program mode high voltage input function.

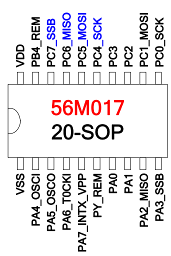


ps: The pad location is for reference only. Please do not apply it to PCB layout.

14SOP Pin Assignment **16SOP Pin Assignment** **20SOP Pin Assignment**







1. Memory Mapping

Address	Content	Comment
0000h - 002Fh	Special Register	
0030h - 007Fh	Reserved	
0080h - 00FFh	Mapping To 1800h - 187Fh	Data RAM
0100h - 01AFh	Mapping To 1800h - 18AFh	Stack
01B0h - 07FFh	Reserved	
0800h - 0FFFh	Mapping To 1800h - 1FFFh Low Nibble	0Xh
1000h - 17FFh	Mapping To 1800h - 1FFFh High Nibble	0Xh
1800h - 18AFh	General Purpose RAM	176B
18B0h - 1FFFh	Reserved	
2000h - 3FFFh	Mapping To C000h - DFFFh	8KB (Read / Write)
4000h - 7FFFh	Reserved	
8000h - BFFFh	Reserved	
C000h - DFEFh	Program MTP ROM	8KB (Read only)
E000h - FFEFh	Program MTP ROM	8KB - 16B (Read only)
FFF0h - FFF7h	System Configure ROM	System area*
FFF8h - FFF9h	Code Option	
FFFAh - FFFBh	Reserved	
FFFCh - FFFDh	Reset Vector	
FFFEh - FFFFh	IRQ Vector	

2. RAM Mapping

Logical Address			Size	Physical Address	Comment
0080h - 00FFh	0100h - 017Fh	1800h - 187Fh	128B	1800h - 187Fh	For zero page RAM and Stack (sharing)
0180h - 01AFh		1880h - 18AFh	48B	1880h - 18AFh	For Data RAM and Stack (sharing)

3. Code Option

Address	b7	b6	b5	b4	b3	b2	b1	b0
FFF8h	-	-	-	-	-	-	-	**OMS0**
FFF9h	-	-	-	-	-	-	-	**PROTB**

OMS0: Main oscillator mode select

0= XT8M 1= BR8M

OMS0	Main Oscillator Mode	Pad Function	
		PA4_OSCI	PA5_OSCO
0	XT8M	OSCI	OSCO
1	BR8M	PA4	PA5

PROTB(FFF9h.0): Protect program ROM option

0: Program ROM is protected. Enter program mode can not read ROM from program data pin but the Code Option bytes data can still read out even **PROTB**=0. Data can write into both program ROM and Code Option bytes except **PROTB** bit.

1: Program ROM is unprotected. Enter program mode can read ROM from program data pin.

4. Special Registers

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
00h	TEST	-	Reserved	-	-	-	-	-	-	-	-	---- ----
01h	PA	R/W	PA Data Reg.	PAD[7:0]								1111 1111
02h	PAWAKE	R/W	Wakeup Mask Reg.	PAW[7:2]						PAW[1:0]		0000 0000
04h	PADIR	R/W	PA Direction Reg.	-	PAC[6:2]					PAC[1:0]		-111 1111
05h	PB	R/W	PB Data Reg.	-	PYD	-	PBD4	-	-	-	-	-0-1 ----
06h	PBTYPE	R/W	PB Output Type Reg.	-	PYC	-	PBT4	-	-	-	-	-1-0 ----
07h	PC	R/W	PC Data Reg.	PCD[7:0]								1111 1111
08h	PCDIR	R/W	PC Direction Reg.	PCC[7:0]								1111 1111
0Ch	PADF0	R/W	Pad Function CTRL 0 Reg.	-	IROS	-	IRS1	IRS0	PA7S	-	-	-0-0 00--
0Dh	PADF1	R/W	Pad Function CTRL 1 Reg.	-	-	-	PA1 PHS	-	-	-	-	---0 ----
0Eh	IER	R/W	Interrupt Enable Reg.	-	-	INTX	PAI	-	TMR1 I	TMR0 I	DIVI	--00 -000
0Fh	IFR	R/W	Interrupt Request Flag Reg.	-	-	INTF	PAF	-	TMR1 F	TMR0 F	DIVF	--00 -000
10h	TMR0	R/W	Timer 0 Data Reg.	TMR0[7:0]								xxxx xxxx
12h	TMR1	R/W	Timer 1 Data Reg.	TMR1[7:0]								xxxx xxxx
16h	TMRC	R/W	Timer Control Reg.	-	T0 SEL	-	-	-	-	TMR1 ON	TMR0 ON	-0-- --00
17h	TMCLK	R/W	Timer Clock Reg.	-	-	-	-	-	TMR1 S0	TMR0 S1	-	---- -xx-
18h	DIVC	R/W	Divider Control Reg.	-	TMR_ SYNC	-	-	-	-	DIVS1	DIVS0	-0-- --xx
1Dh	SYSCLK	R/W	System Clock Select Reg.	-	F4M SEL	-	RCS0	-	-	-	-	-1-1 ----
1Eh	HALT	W	CPU HALT Control Reg.									xxxx xxxx
2Dh	OPC0	R/W	OP/COMP Control 0 Reg.	RPUS[1:0]		GAINS[1:0]		IRFLT[1:0]		VREFS[1:0]		1001 1010
2Eh	OPC1	R/W	OP/COMP Control 1 Reg.	OPO	OPIS0	OPI	OPIF	OPON	OPOS	OPIS1	IRTO	x000 0x00
2Fh	MF	R/W	Miscellaneous Function Reg.	MCB[5:0]						-	-	1000 00--
32h	SPCR	R/W	SPI Control Reg.	SPII	SPE	DORD	MSTR	CPOL	CPHA	SPIR1	SPIR0	0000 0000
33h	SPSR	R/W	SPI Status Reg.	SPIF	WCOL	-	-	MSSB D	-	SPIS	SPI2X	00-- 1-x0
34h	SPDR	R/W	SPI Data Reg.	SPD[7:0]								xxxx xxxx
3Ah	PAK	R/W	PA Key Scan Control Reg.	PAK7	PAK6	PAK5	PAK4	PAK3	PAK2	PAK1	PAK0	xxxx xxxx
3Bh	PBK	R/W	PB Key Scan Control Reg.	KSEN	PYK	-	-	KSPW[1:0]		KSPNO[1:0]		0x-- xxxx
3Ch	PCK	R/W	PC Key Scan Control Reg.	PCK7	PCK6	PCK5	PCK4	PCK3	PCK2	PCK1	PCK0	xxxx xxxx
3Dh	LVC	R/W	Low Voltage Control Reg.	EN LVD	-	LVDS	LVDF	LVRF	-	-	-	0-x0 1---
3Eh	FUSE	R	Fuse Reg.	FSA[5:0]						-	-	aaaa aa--*1
4Fh	WS	R	Wait State Select Reg.	-	-	-	-	-	-	WR FAIL	BUSY	---- --00

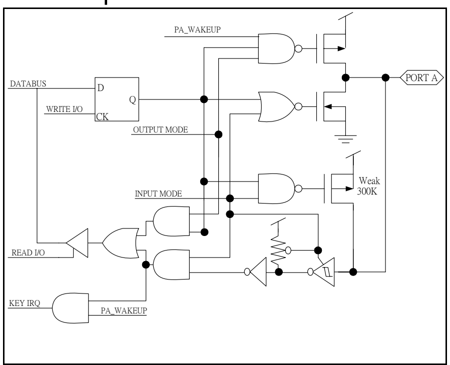
*1: FSA[5:0] POR value: Determined by wafer CP or Writer data.

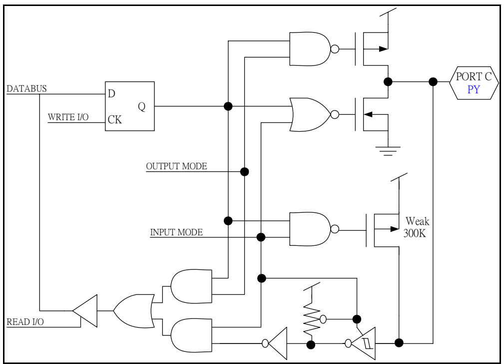
5. Port A, Port B, Port C

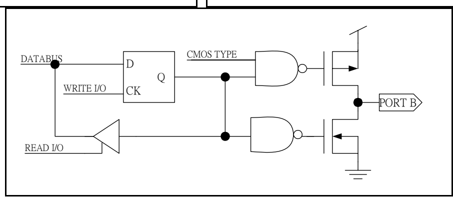
ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
01h	PA	R/W	PA Data Reg.	**PAD[7:0]**								1111 1111
02h	PAWAKE	R/W	Wakeup Mask Reg.	**PAW[7:2]**						**PAW[1:0]**		0000 0000
04h	PADIR	R/W	PA Direction Reg.	-	**PAC[6:2]**					**PAC[1:0]**		-111 1111
05h	PB	R/W	PB Data Reg.	-	**PYD**	-	**PBD4**	-	-	-	-	-0-1 ----
06h	PBTYPE	R/W	PB Output Type Reg.	-	**PYC**	-	**PBT4**	-	-	-	-	-1-0 ----
07h	PC	R/W	PC Data Reg.	**PCD[7:0]**								1111 1111
08h	PCDIR	R/W	PC Direction Reg.	**PCC[7:0]**								1111 1111

ADR	Register	Read		Write		Comment
01h/05h/07h	PA/PB/PC	I/P	Pad Data	0: Selected Tri-state 1: Selected Pull-High		PA7 is input only PB used as output only
		O/P	Register Data	0: output logic Low 1: output logic High		
02h	PAWAKE	Register Data		PA=I/P	0: bit n is none wakeup 1: bit n is wakeup	1 → 0 (Falling edge) Wakeup
				PA=O/P	0: bit n is NMOS Output Port 1: bit n is CMOS Output Port	
06h.4	PBTYPE	Register Data		0: bit n is NMOS Output Port 1: bit n is CMOS Output Port		NMOS or CMOS for output port
04h/06h.6/08h	PADIR/ PBTYPE/PCDIR	Register Data		0: bit n is Output Port 1: bit n is Input Port		PC & PY output mode is CMOS only.

Note: 1. PB4 is an output only port. PBT4 defines PB4 output type is CMOS or NMOS.
2. PY is an I/O port. PYC controls PY I/O direction.







I/O Port Summary

	Input Function			Output Function	
	Pull-High	Tri-state	Wakeup	CMOS	NMOS
PA[6:0]	V	V	V	V	V
PA7	V	V	V	-	-
PB	-	-	-	V	V
PC	V	V	-	V	-
PY	V	V	-	V	-

The Pull-High supply voltage must <VDD+0.7V when NMOS Open-drain output.

Pad Function Definition

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
0Ch	PADF0	R/W	Pad Function CTRL 0 Reg.	-	**IROS**	-	**IRS1**	**IRS0**	**PA7S**	-	-	-0-0 00--
0Dh	PADF1	R/W	Pad Function CTRL 1 Reg.	-	-	-	**PA1 PHS**	-	-	-	-	---0 ----
16h	TMRC	R/W	Timer Control Reg.	-	**T0 SEL**	-	-	-	-	TMR1 ON	TMR0 ON	-0-- --00
2Eh	OPC1	R/W	OP/COMP Control 1 Reg.	OPO	OPIS0	OPI	OPIF	OPON	OPOS	OPIS1	**IRTO**	x000 0x00
32h	SPCR	R/W	SPI Control Reg.	SPII	**SPE**	DORD	MSTR	CPOL	CPHA	SPIR1	SPIR0	0000 0000
33h	SPSR	R/W	SPI Status Reg.	SPIF	WCOL	-	-	MSSBD	-	**SPIS**	SPI2X	00-- 1-x0

I/O Port Operating Mode Select

PAD Name	Register Bit		Pad Function	Note
PA7_INTX_VPP	**PA7S**	0	PA7	
		1	INTX	External interrupt pin, falling edge trigger
		X	VPP	PA7_INTX_VPP > 5V will enter program mode.
PA6_T0CKI	**T0SEL**	0	PA6	
		1	T0CK I	T0CKI input
PA5_OSCO	**OMS0** **(FFF8h.0)**	0	OSCO	
		1	PA5	
PA4_OSCI	**OMS0** **(FFF8h.0)**	0	OSCI	
		1	PA4	
PA3_SSB, PA2_MISO	**SPIS, SPE**	00 or 1X	PA[3:2]	
		01	SSB, MISO	SPI SSB and MISO function
PA1	**PA1PHS**	0	PA1	Pull-high R=300K Ohm if PA1 set as input with pull-high R.
		1	PA1	Pull-high R=10K Ohm if PA1 set as input with pull-high R.
PA0_OPO	**IRTO**	0	PA0	
		1	OPO	
PB4_REM	**IROS, IRS1, IRS0**	0XX	PB4	I_{OL}=6mA @ V_{OL}=0.3V
		100	PB4	I_{OL}=320mA @ V_{OL}=1.5V
		101	PB4	
		110	TMR0/2 (1/2 duty)	IR output, I_{OL}=320mA @ V_{OL}=1.5V
		111	TMR0/3 (1/3 duty)	
PY_REM	**IROS, IRS1, IRS0**	000	PY	
		001	PY	
		010	TMR0/2 (1/2 duty)	IR output
		011	TMR0/3 (1/3 duty)	
		1XX	PY	
PC7_SSB, PC6_MISO, PC5_MOSI, PC4_SCK	**SPIS, SPE**	0X or 10	PC[7:4]	
		11	SSB, MISO, MOSI, SCK	SPI SSB, MISO, MOSI and SCK function
PC1_MOSI, PC0_SCK	**SPIS, SPE**	00 or 1X	PC[1:0]	
		01	MOSI, SCK	SPI MOSI and SCK function

6. MTP ROM Write

ADR	NAME	R/W	Content	b7	b6	b5	B4	b3	b2	b1	b0	Value on POR
4Fh	WS	R	Wait State Select Reg.	-	-	-	-	-	-	**WRFAIL**	**BUSY**	---- --00

BUSY: MTP ROM write busy flag

0 = No write operation is running 1 = Write operation is running

WRFAIL: MTP ROM write pass or fail flag

0 = No write operation is failed 1= Write operation is failed

BUSY and **WRFAIL** flags are read only. The two flags are used for checking lower 8KB (C000h - DFFFh) MTP write status. While the data is writing into the lower 8KB MTP ROM, **BUSY** flag will set. When **BUSY**=1, user can access the upper 8KB (E000h - FFFFh) MTP ROM but can not access the lower 8KB MTP ROM until the write operation is completed. After MTP write operation is completed, hardware will clear the **BUSY** flag automatically. The MTP typical write time, Twr, is 1ms @ 3.3V.

If write operation is failed, the **WRFAIL** flag will be set and the **BUSY** flag will be cleared at the same time. User can try to write the same location of the MTP ROM again for it may be successful at the second write.

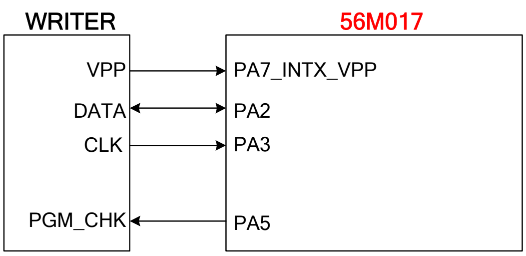
MTP Program Mode

PA7_INTX_VPP pin force high voltage, 8V, will enter program mode. PA5 is used for check the program mode is in progress or not. Force PA7_INTX_VPP pin to VDD can leave program mode and the hardware will generate another one shot pulse to reset the chip again. In program mode, PA3 is used for clock input pin and PA2 is used as data in/out pin.

MTP ROM Program Mode

PAD Name	Normal Mode	Program Mode
PA7_INTX_VPP	PA7_INTX_VPP < 5V	PA7_INTX_VPP (Typ. 8V) > 5V
PA2	PA2	I/O pin for program data transfer.
PA3	PA3	Input pin with pull-high for program clock inputs.
PA5	PA5	Output pin. Clock signal is output to PA5 for writer check.

Program Mode Application Block Diagram



7. Oscillator, Fosc & Fcpu

ADR	NAME	R/W	Content	b7	b6	b5	B4	b3	b2	b1	b0	Value on POR
1Dh	SYSCLK	R/W	System Clock Select Reg.	-	**F4M SEL**	-	**RC S0**	-	-	-	-	-1-1 ----
2Fh	MF	R/W	Miscellaneous Function Reg.	**MCB[5:0]**						-	-	1000 00--

RCS0: Fsys-Clock select

0: Fsys=Fosc/1 1: Fsys=Fosc/2

F4MSEL: F4M select

0: F4M=Fosc/1 ***1: F4M=Fosc/2***

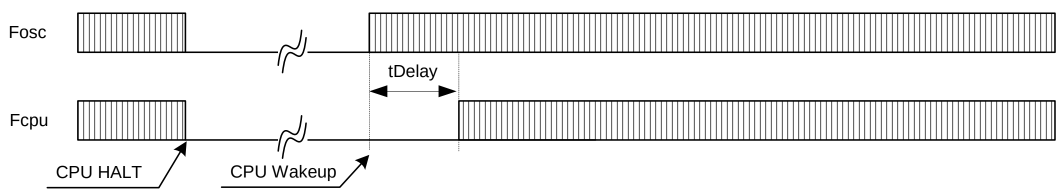
OMS0 (FFF8h.0)	PA5_OSCO, PA4_OSCI PAD Function	Fosc Mode
0	OSCO, OSCI	XT mode
1	PA5, PA4	BR mode

MCB[5:0]: Main-clock calibration bits

MCB[5:0]	Adjust Percentage	Frequency After Adjusted
00h	+32%	Fosc = Forg x (1+0.32)
001	+31%	Fosc = Forg x (1+0.31)
…	…	
1Fh	+1%	Fosc = Forg x (1+0.01)
20h	***0%***	***Fosc = Forg (Forg is non-adjusted freq. Target is 8MHz.)***
21h	-1%	Fosc = Forg x (1-0.01)
22h	-2%	Fosc = Forg x (1-0.02)
…		
3Fh	-31%	Fosc = Forg x (1-0.31)

Fcpu Timing Diagram

Fcpu=Fsys



tDelay:

tDelay = 4Fcpu (BR8M) or 1024Fosc (XT8M)

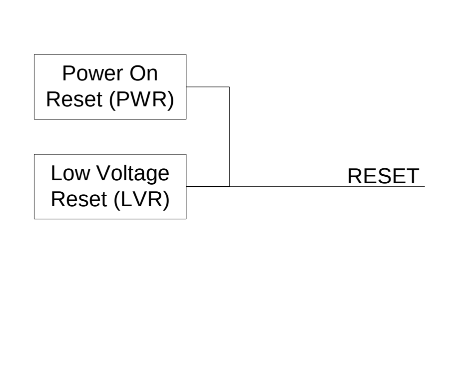
8. Fuse Register

ADR	NAME	R/W	Content	b7	b6	b5	B4	b3	b2	b1	b0	Value on POR
3Eh	FUSE	R	Fuse Reg.	FSA[5:0]						-	-	aaaa aa--*1

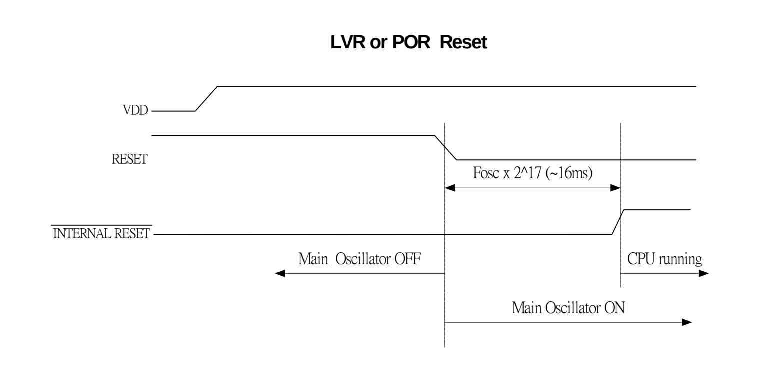
*1: **FSA[5:0]** POR value: Determined by wafer CP or Writer data.

FSA[5:0]: BR8M oscillator calibration bits. The **FSA[5:0]** are programmed at wafer CP or Writer data. User can load **FSA[5:0]** then write to **MCB[5:0]** to get high accuracy BR8M frequency.

9. RESET



RESET Block Diagram



Reset Timing Diagram

10. Low Voltage Control Register

ADR	NAME	R/W	Content	b7	B6	b5	B4	b3	b2	b1	b0	Value on POR
3Dh	LVC	R/W	Low Voltage Control Reg.	**EN LVD**	-	**LVDS**	**LVDF**	**LVRF**	-	-	-	0-x0 1---

LVRF: Power-on or low voltage reset flag

0: Cleared by software 1: VDD < LVR level

While VDD < LVR level, the **LVRF** is set to logic high. Otherwise the **LVRF** keeps un-changed. When **LVRF**=1, it must be cleared by software for next time checking. **LVRF** cannot be set to '1' by software. LVR function is always enabled. The LVR voltage level is 1.65V +/- 10% with Vh=0.1V.

LVDF: Low voltage detect flag

0: VDD > LVD level 1: VDD < LVD level

Note: **LVDF** is a read only flag.

LVDS: LVD detect level select

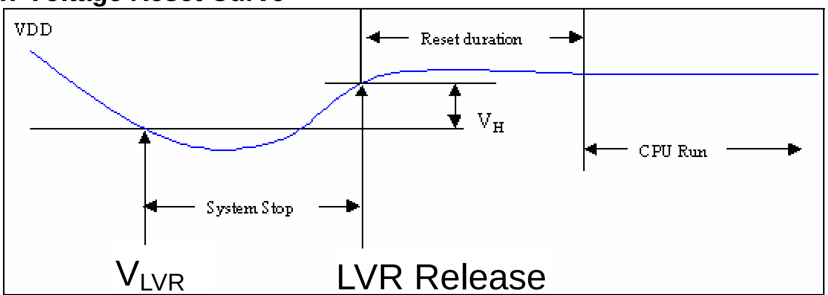
0: LVD=2.05V 1: LVD=2.25V

ENLVD: LVD function enable bit

0= LVD function disabled 1= LVD function enabled

Note: LVR function is always enabled. V_{LVR} = 1.65V ±10%, V_H = 0.1V. I_{LVR} = 1.0uA @ V_{DD}=3V.

Low Voltage Reset Curve



11. CPU HALT

ADR	NAME	R/W	Content	b7	b6	b5	B4	b3	b2	b1	b0	Value on POR
1Eh	HALT	W	CPU HALT Control Reg.									xxxx xxxx

When writing into address HALT, CPU will go into sleep mode.

When in sleep mode, all kinds of interrupt sources can wake up CPU, but IER need to be set to '1'.

CPU Operating Mode

CPU Operating Mode	Actions	Clock Status		Note
		Fcpu	Fosc	
Sleep	1. Write the HALT register	OFF	OFF	Turn-off all and I_{stb}<1uA
Normal	1. Wakeup from HALT state 2. Start from RESET	Fsys	ON	Normal speed.

Note: The Fcpu will be turned off after write HALT register.

12. Divider

The Divider can be used as time base or clock input sampling rate.

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
18h	DIVC	R/W	Divider Control Reg.	-	TMR_SYNC	-	-	-	-	DIVS1	DIVS0	-0-- --xx

DIVS1	DIVS0	Divider Clock
0	0	F4M/128/4 (8KHz)
0	1	F4M/128/2 (16KHz)
1	0	F4M/128/64 (512Hz)
1	1	F4M/128/32 (1KHz)

13. Timer 0,1

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
10h	TMR0	R/W	Timer 0 Data Reg.	**TMR0[7:0]**								xxxx xxxx
12h	TMR1	R/W	Timer 1 Data Reg.	**TMR1[7:0]**								xxxx xxxx
16h	TMRC	R/W	Timer Control Reg.	-	**T0 SEL**	-	-	-	-	**TMR1 ON**	**TMR0 ON**	-0-- --00
17h	TMCLK	R/W	Timer Clock Reg.	-	-	-	-	-	**TMR1 S0**	**TMR0 S1**	-	---- -xx-
18h	DIVC	R/W	Divider Control Reg.	-	**TMR_ SYNC**	-	-	-	-	**DIVS1**	**DIVS0**	-0-- --xx

TMR0[7:0]: Timer 0 data register.

TMR1[7:0]: Timer 1 data register.

TMR0ON: 1= Timer 0 ON ***0= Timer 0 OFF***

TMR1ON: 1= Time 1 ON ***0= Timer 1 OFF***

T0SEL: TMR0 clock source select

0= T0I = F4M4 1= T0I = T0CKI

Note: T0CKI is falling edge trigger.

TMR_SYNC: TMR0 & TMR1 ON/OFF sync control bit

0= Asynchronous 1= Sync with DIV

While **TMR_SYNC**=1, the TMR0 & TMR1 are synchronized by DIV. Set/clear **TMR1ON** and **TMR0ON**, TMR1 and TMR0 will not start/stop counting until DIV occurs.

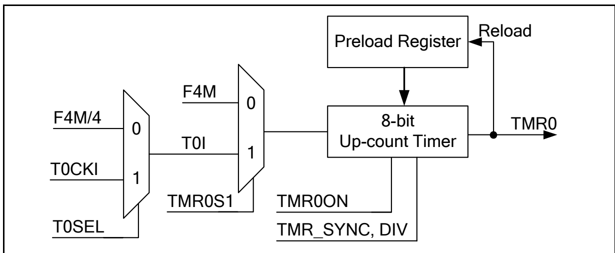
TMR0S1: TMR0 clock source select

0= F4M 1= T0I

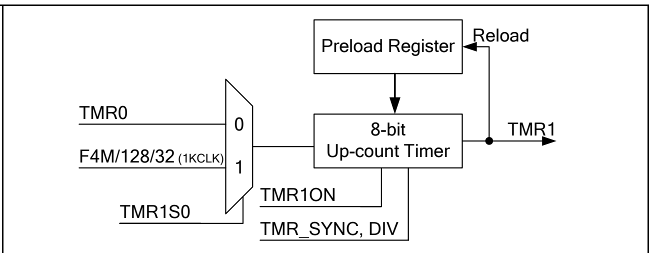
TMR1S0: TMR1 clock source select

0= TMR0 1= F4M/128/32$_{(1KCLK)}$

Timer 0, 1 are up-count timers. When time out (FFh → 00h) will set TMRF flag, request IRQ interrupt and reload the initial value from Preload Register at same time.
When Timer 0, 1 are off that Data write to Preload Register & Timer. When time is on Data write to Preload Register, until time out that data write to timer from Preload register.



Timer 0



Timer 1

14. IR Output Function

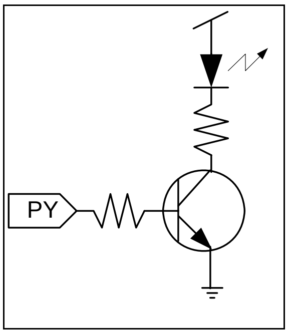
ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
0Ch	PADF0	R/W	Pad Function CTRL 0 Reg.	-	**IROS**	-	**IRS1**	**IRS0**	PA7S	-	-	-0-0 00--

A. IR output from PY

PY can be used as IR output pin. It is high-active.

The PY is input tri-state at POR initial.

The application circuit is shown as in the right diagram.



IROS	IRS1	IRS0	Pad Function
0	0	0	PY
0	0	1	PY
0	1	0	IR output (TMR0/2, 1/2 duty)
0	1	1	IR output (TMR0/3, 1/3 duty)
1	X	X	PY

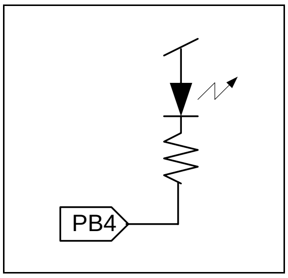
The carrier output sequences are

a. PY set to CMOS output and output ‘0’.
b. **IROS** cleared as ‘0’.
c. **IRS[1:0]**=10 or 11 for active IR carrier output. (PY output low while TMR0 off.)
d. **IRS1**=0 for in-active IR carrier output.

B. IR output from PB4

The PB4 can be used as IR output pin. It is low-active.

The application circuit is show as in right diagram.

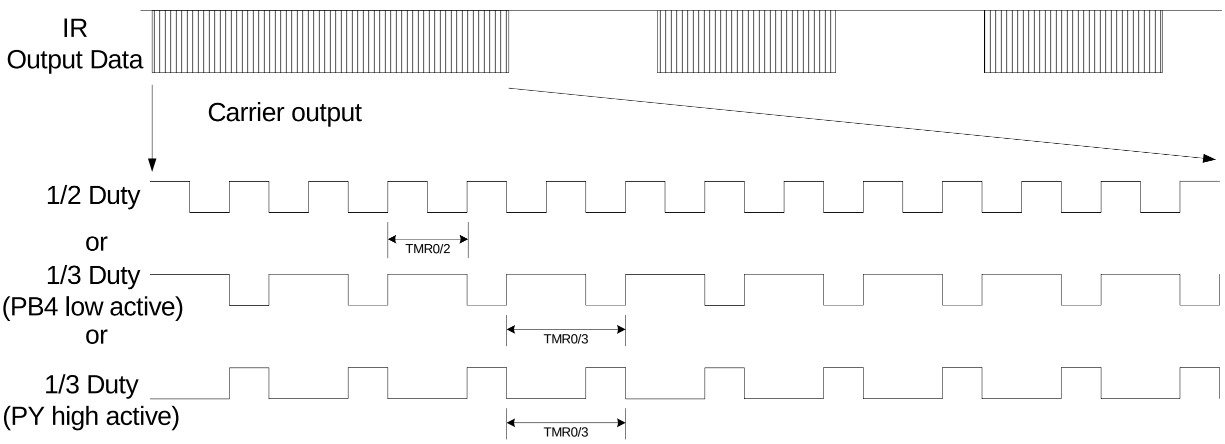


IROS	IRS1	IRS0	Pad Function
0	X	X	PB4, I_{OL}=6mA @ V_{OL}=0.3V
1	0	0	PB4, I_{OL}=320mA @ V_{OL}=1.5V
1	0	1	PB4, I_{OL}=320mA @ V_{OL}=1.5V
1	1	0	IR output (TMR0/2, 1/2 duty), I_{OL}=320mA @ V_{OL}=1.5V
1	1	1	IR output (TMR0/3, 1/3 duty), I_{OL}=320mA @ V_{OL}=1.5V

The carrier output sequences are

I. **IROS** set to ‘1’.
II. **IRS[1:0]**=10 or 11 for active IR carrier output. (PB4 output high while TMR0 off.)
III. **IRS1**=0 for in-active IR carrier output.

The IR carrier duty is 1/2 in frequency out from TMR0/2, the other is 1/3 and out from TMR0/3. The output waveform is show as below.



15. IR Learning Function

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
2Dh	OPC0	R/W	OP/COMP Control 0 Reg.	RPUS[1:0]		GAINS[1:0]		IRFLT[1:0]		VREFS[1:0]		1001 1010
2Eh	OPC1	R/W	OP/COMP Control 1 Reg.	OPO	OPIS0	OPI	OPIF	OPON	OPOS	OPIS1	IRTO	x000 0x00

RPUS[1:0]: Input resistor select
00: R_H = 0.85Rx 01: R_H = 1.15Rx ***10: R_H = Rx*** 11: R_H = 0.7Rx

GAINS[1:0]: OP1 gain select
00: Gain = 2 ***01: Gain = 3*** 10: Gain = 4 11: Gain = 5

IRFLT[1:0]: IR input digital filter select
00 = 20ns 01 = 40ns ***10 = 80ns*** 11 = 150ns

VREFS [1:0]: COMP reference voltage select
00: Vref=VDD-0.5Vx 01: Vref=VDD-0.4Vx ***10: Vref=VDD-0.3Vx*** 11: Vref=VDD-0.2Vx

OPO: IR output data (Read only)

OPIS[1:0]: OPO interrupt select
00 = OPO falling edge interrupt 01 = OPO rising edge interrupt
1X = OPO falling and rising edge interrupt

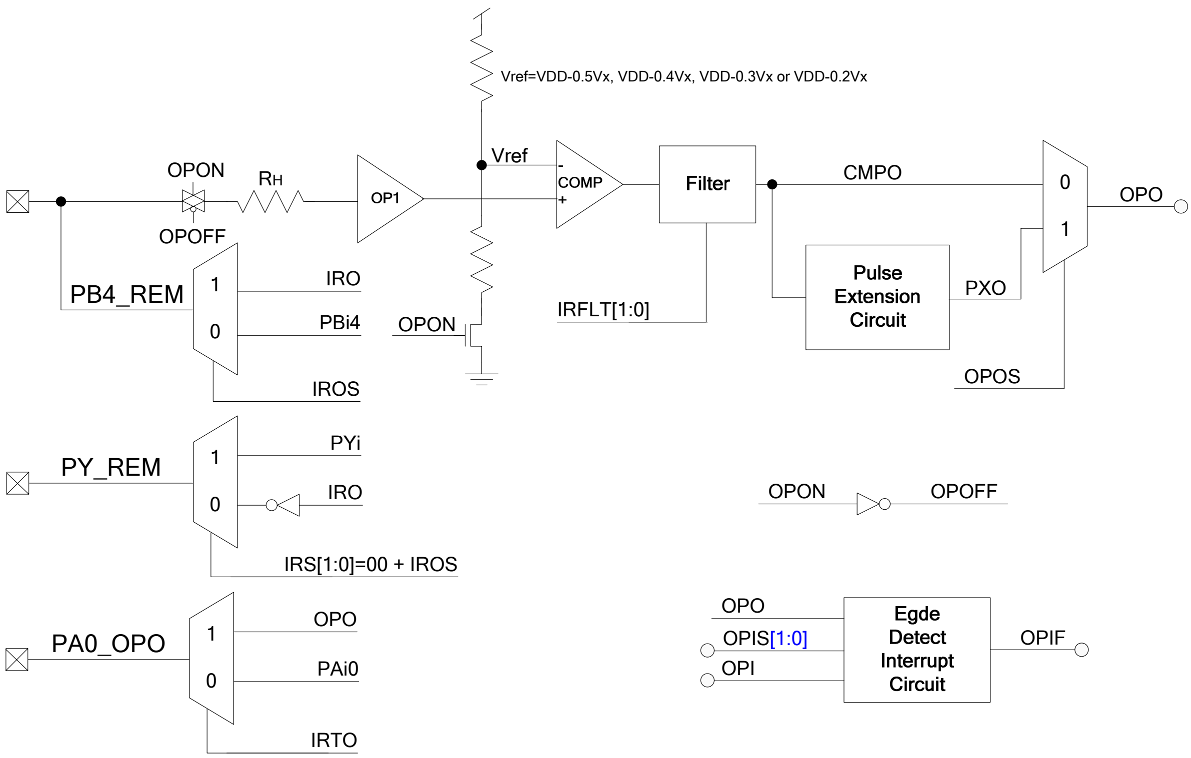
OPI: OPO interrupt enable bit
0 = Disable OPO interrupt 1 = Enable OPO interrupt

OPIF: OPO interrupt flag bit
0 = No OPO interrupt occurs 1 = OPO interrupt occurs

OPON: OP ON/OFF bit
0 = OP OFF 1 = OP ON

OPOS: OP output select
0: OPO = CMPO 1: OPO = PXO
Pulse Extension Circuit is used to extend CMPO pulse to guarantee each PXO output low pulse width greater than 8us. If CMPO low pulse width less than 8us, the PXO low pulse width will be 8us. If CMPO low pulse width larger than 8us, the PXO follows the CMPO output.

IRTO: IR learning output to pad select
0 = OPO can not output to pad 1 = OPO can output to PA0 pad



16. Interrupt

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
0Eh	IER	R/W	Interrupt Enable Reg.	-	-	**INTX**	**PAI**	-	**TMR1I**	**TMR0I**	**DIVI**	--00 -000
0Fh	IFR	R/W	Interrupt Request Flag Reg.	-	-	**INTF**	**PAF**	-	**TMR1F**	**TMR0F**	**DIVF**	--00 -000
2Eh	OPC1	R/W	OP/COMP Control 1 Reg.	OPO	OPIS	**OPI**	**OPIF**	OPON	OPOS	-	IRTO	x000 0x-0
32h	SPCR	R/W	SPI Control Reg.	**SPII**	SPE	DORD	MSTR	CPOL	CPHA	SPIR1	SPIR0	0000 0000
33h	SPSR	R/W	SPI Status Reg.	**SPIF**	WCOL	-	-	MSSBD	-	SPIS	SPI2X	00-- 1-x0

IER bit n=1: Enable interrupt

IER bit n=0: Disable interrupt

- ✧ **DIVI**: Divider interrupt
- ✧ **TMR0I**: Timer 0 interrupt
- ✧ **TMR1I**: Timer1 interrupt, for real time clock
- ✧ **PAI**: Port A wakeup interrupt
- ✧ **INTX**: External input interrupt from PA7
- ✧ **OPI**: OPO edge trigger interrupt
- ✧ **SPII**: SPI interrupt

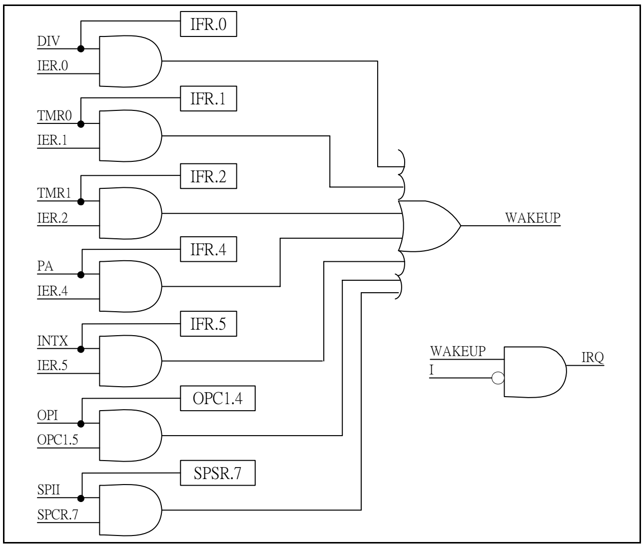
When interrupt happened, the relative IFR will be set to '1'. If IER is set to enable the interrupt, it will request to go into interrupt service routines. Before it goes into Interrupt Service Routine (ISR), the hardware will automatically set the I* bit to '1' to prevent interrupt from occurring again. Within ISR, user needs to judge from IFR to decide which kind of interrupts. Once it is decided, IFR needs to be clear to 0 by program.

If there are two interrupt source requests happening simultaneously, the priority should be decided by program. When the first interrupt request is done from RTI, the next interrupt will happening right away. These procedures should be repeated until all interrupts are taking care. User could 'CLI' in ISR for enable nest interrupt.

PS: The 'I bit' is a global interrupt mask bit, set by 'SEI', clear by 'CLI'.

EX.

```
.page0
IFRBuf          DS      1           ;use in ISR only
.ends
.code
IRQ:
                PHA
                LDA     IER
                AND     IFR
                STA     IFRBuf
                BBS1    IFRBuf, tmr0irq
                BBS2    IFRBuf, tmr1irq
                BBS0    IFRBuf, divirq
                BBS4    IFRBuf, pairq
                BBS6    IFRBuf, lcdirq
                BRA     extirq
divirq:
                RMB0    IFR
                ……
                BRA     extirq
tmr0irq:
                RMB1    IFR
                ……
                BRA     extirq
……
lcdirq:
                RMB1    IFR
                ……
extirq:
                PLA
                RTI
.ends
```



17. SPI Function

ADDR	NAME	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
32h	SPCR	SPI Control Reg.	SPII	**SPE**	**DORD**	**MSTR**	**CPOL**	**CPHA**	**SPIR1**	**SPIR0**	0000 0000
33h	SPSR	SPI Status Reg.	SPIF	**WCOL**	-	-	**MSSBD**	-	**SPIS**	**SPI2X**	00-- 1-x0
34h	SPDR	SPI Data Reg.	**SPD[7:0]**								xxxx xxxx

SPE: SPI enable
0 = Disable 1 = Enable

SPIS: SPI interface pins select
0 = PA3_SSB, PA2_MISO, PC1_MOSI, PC0_SCK are selected
1 = PC7_SSB, PC6_MISO, PC5_MOSI, PC4_SCK are selected

DORD: SPI data order
0 = MSB transmitted first 1 = LSB transmitted first

MSTR: SPI master/slave select
0 = Slave 1 = Master

CPOL: SPI clock polarity
0 = Normal low when idle 1 = Normal high when idle

CPHA: SPI clock phase
0 = Leading edge sampling 1 = Trailing edge sampling

CPOL and CPHA Functionality

SPI Mode	CPOL	CPHA	Leading Edge	Trailing Edge
0	0	0	Sample (Rising)	Setup (Falling)
1	0	1	Setup (Rising)	Sample (Falling)
2	1	0	Sample (Falling)	Setup (Rising)
3	1	1	Setup (Falling)	Sample (Rising)

SPIR[1:0]: SPI clock rate select

SPI2X: Double SPI speed select

	SCK Frequency	
SPIR[1 :0]	**SPI2X=0**	**SPI2X=1**
00	Fosc / 2	Fosc / 1
01	Fosc / 8	Fosc / 4
10	Fosc / 32	Fosc / 16
11	Fosc / 64	Fosc / 32

MSSBD: SPI Master mode SSB output data.
While configured as SPI Master and **SPE**=1, PA3_SSB or PC7_SSB pin will be as SPI Master SSB output. The output data of SSB pin refers to **MSSBD** register bit setting. **MSSBD**=1 SSB pin output high and **MSSBD**=0 SSB pin output low. While configured as SPI Slave or **SPE**=0, the register bit is ignored.

WCOL: SPI write collision flag. This bit is read only.
The **WCOL** bit is set if the SPI Data Register (SPDR) is written during a data transfer. The **WCOL** bit is cleared by first reading the SPI Status Register with **WCOL** set, and then accessing the SPI Data Register.

SPD[7:0]: SPI data
The SPI Data Register is a Read/Write Register used for data transfer between the register file and the SPI Shift Register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

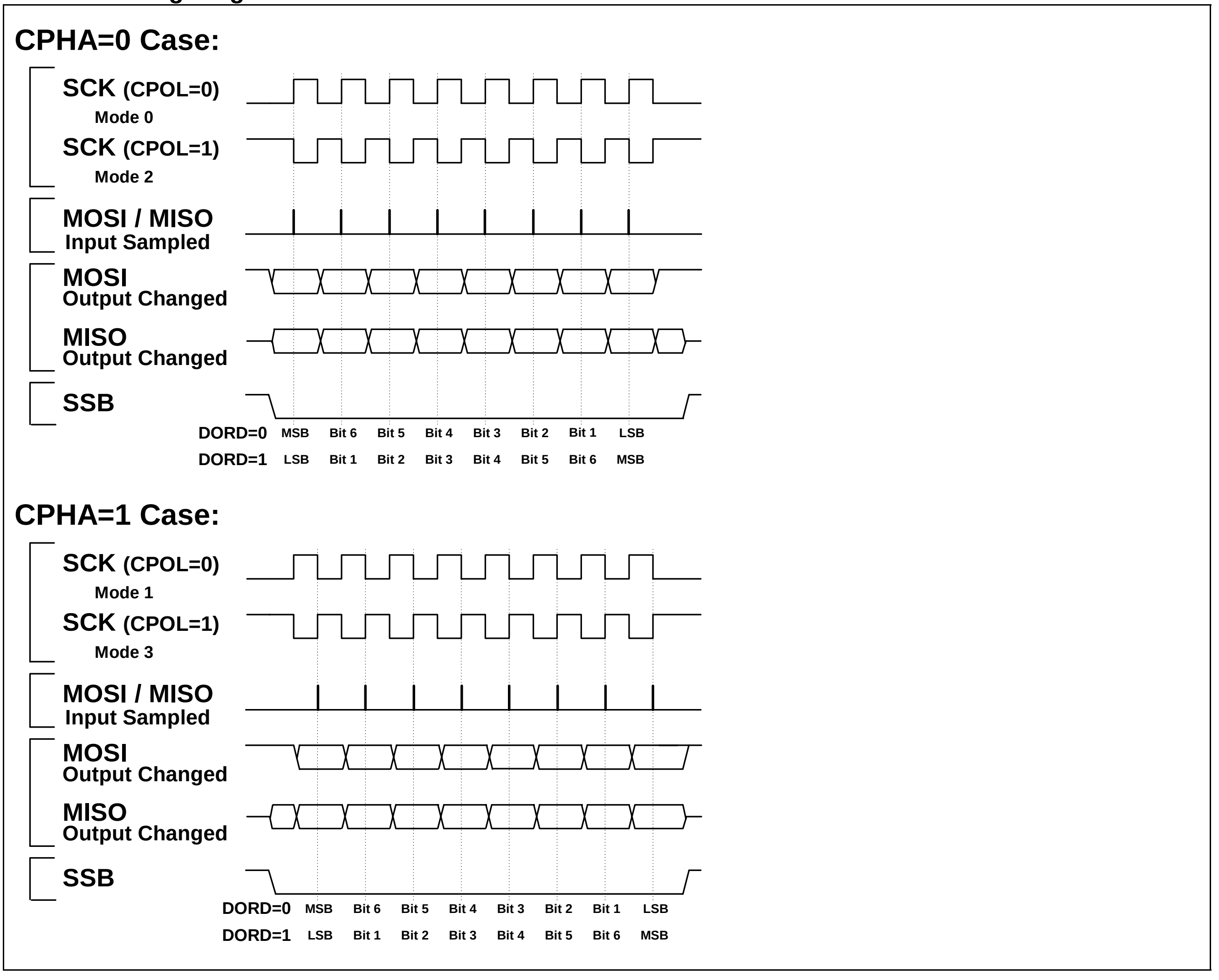
SPI Function Description

When configured as a Master, the SPI interface has no automatic control of the SSB line. This must be handled by user software before communication can start. When this is done, writing a byte to the SPI Data Register starts the SPI clock generator, and the hardware shifts the 8 bits into the Slave. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (**SPIF**). If the SPI interrupt enable bit (**SPII**) in the SPCR Register is set, an interrupt is requested. The Master may continue to shift the next byte by writing it into SPDR, or signal the end of packet by driving high the Slave Select, SSB line. The last incoming byte will be kept in the buffer register for later use.

When configured as a Slave, the SPI interface will remain sleeping with MISO tri-stated as long as the SSB pin is driven high. In this state, software may update the contents of the SPI Data Register, SPDR, but the data will not be shifted out by incoming clock pulses on the SCK pin until the SSB pin is driven low. As one byte has been completely shifted, the end of transmission flag (**SPIF**) is set. If the SPI interrupt enable bit (**SPII**) in the SPCR Register is set, an interrupt is requested. The Slave may continue to place new data to be sent into SPDR before reading the incoming data. The last incoming byte will be kept in the buffer register for later use.

The system is single buffered in the transmit direction and double buffered in the receive direction. This means that bytes to be transmitted can not be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received character must be read from the SPI Data Register before the next character has been completely shifted in. Otherwise, the first byte is lost.

SPI Timing Diagram



18. Key Scan Function

ADR	NAME	R/W	Content	b7	b6	b5	b4	b3	b2	b1	b0	Value on POR
3Ah	PAK	R/W	PA Key Scan Control Reg.	**PAK7**	**PAK6**	**PAK5**	**PAK4**	**PAK3**	**PAK2**	**PAK1**	**PAK0**	xxxx xxxx
3Bh	PBK	R/W	PB Key Scan Control Reg.	**KSEN**	**PYK**	-	-	**KSPW[1:0]**		**KSPNO[1:0]**		0x-- xxxx
3Ch	PCK	R/W	PC Key Scan Control Reg.	**PCK7**	**PCK6**	**PCK5**	**PCK4**	**PCK3**	**PCK2**	**PCK1**	**PCK0**	xxxx xxxx

KSEN: Key scan function enable bit

0: Disable key scan function 1: Enable key scan function

While **KSEN**=1, the internal BR35K is automatically turned on and starts to oscillation.
While **KSEN**=0, BR35K is turned off immediately. PA[7:0], PY, PC[7:0] are used as normal I/O function. The **PAK7**, **PAK6**, **PAK5**, **PAK4**, **PAK3**, **PAK2**, **PAK1**, **PAK0**, **PYK**, **PCK7**, **PCK6**, **PCK5**, **PCK4**, **PCK3**, **PCK2**, **PCK1** and **PCK0** register bit settings are ignored.

PAK7, **PAK6**, **PAK5**, **PAK4**, **PAK3**, **PAK2**, **PAK1**, **PAK0**: PA[7:0] key scan function select

0: PA used as normal I/O

1: PA used as keyboard scan output line or return line

PAK7, **PAK6**, **PAK5**, **PAK4**, **PAK3**, **PAK2**, **PAK1** and **PAK0** control PA7, PA6, PA5, PA4, PA3, PA2, PA1 and PA0 function respectively.

In key scan mode, i.e. **KSEN**=1, if PAn (n=0~7) is an input only function and **PAKn**=1, PAn is used as keyboard scan return line. If PAn is an I/O function and **PAKn**=1, PAn will output low in its scan cycle and act as keyboard scan return line in the remaining cycles.

PYK: PY key scan function select

0: PY used as normal I/O

1: PY used as keyboard scan output line or return line

In key scan mode, i.e. **KSEN**=1, and **PYK**=1, PY will output low in its scan cycle and act as keyboard scan return line in the remaining cycles.

PCK7, **PAK6**, **PCK5**, **PAK4**, **PCK3**, **PCK2**, **PCK1**, **PCK0**: PC[7:0] key scan function select

0: PC used as normal I/O

1: PC used as keyboard scan output line or return line

PCK7, **PCK6**, **PCK5**, **PCK4**, **PCK3**, **PCK2**, **PCK1** and **PCK0** control PC7, PC6, PC5, PC4, PC3, PC2, PC1 and PC0 function respectively.

In key scan mode, i.e. **KSEN**=1, and **PCKn**=1, PCn will output low in its scan cycle and act as keyboard scan return line in the remaining cycles.

KSPNO[1:0]: Key scan pulse non-overlap select

00: 1 scan pulse width 01: 2 scan pulse width
10: 3 scan pulse width 11: reserved

KSPW[1:0]: Key scan pulse width select

00: 4 Fsub cycle 10: 8 Fsub cycles
10: 16 Fsub cycle 11: 32 Fsub cycles

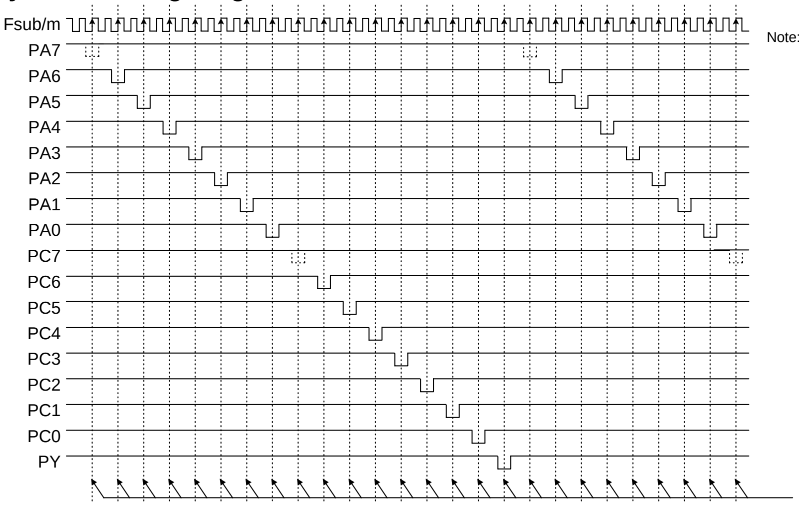
Keyboard scan time table: (Fix 17 scan lines)

KSPW[1:0]		KSPNO[1:0]		Keyboard Scan Cycle Time
0	0	0	0	3.89ms (17 x 4 x 2 x 28.6us)
		0	1	5.83ms (17 x 4 x 3 x 28.6us)
		1	0	7.77ms (17 x 4 x 4 x 28.6us)
0	1	0	0	7.77ms (17 x 8 x 2 x 28.6us)
		0	1	11.7ms (17 x 8 x 3 x 28.6us)
		1	0	15.5ms (17 x 8 x 4 x 28.6us)
1	0	0	0	15.5ms (17 x 16 x 2 x 28.6us)
		0	1	23.3ms (17 x 16 x 3 x 28.6us)
		1	0	31.1ms (17 x 16 x 4 x 28.6us)
1	1	0	0	31.1ms (17 x 32 x 2 x 28.6us)
		0	1	46.6ms (17 x 32 x 3 x 28.6us)
		1	0	62.2ms (17 x 32 x 4 x 28.6us)

Note: The BR35K frequency is 35KHz +/- 30%. 28.6us is its center frequency cycle time.

Key scan output line sequence:
While **KSEN**=1, the key scan output will follow the sequence:
PA7→PA6→PA5→PA4→PA3→PA2→PA1→PA0→PC7→PC6→PC5→PC4→PC3→PC2→PC1→PC0→PY. If some of the pads are used as normal I/O function, act as input only function or do not exist, the scan output low pulse will not generate and the correspondent cycles are replaced by dummy cycles.

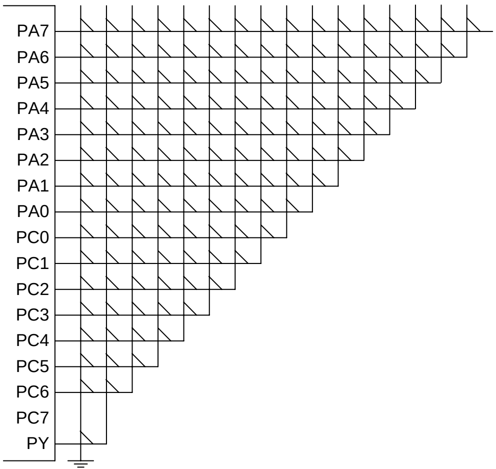
Key Scan Timing Diagram



Note: 1. Fsub/m: m=4 if KSPW[1:0]=00
m=8 if KSPW[1:0]=01
m=16 if KSPW[1:0]=10
m=32 if KSPW[1:0]=11
2. In the case, PA7 is input only and PCK7=0.
3. In the case, KSPNO[1:0]=00.

Keyboard scan return lines latch.

Key Scan Application Diagram



Note: In the case, PA7 is input only. PC7 used as normal I/O (PCK7=0).

19. DC Characteristics

F_{OSC}=8MHz, TA=25℃

Symbol	Parameter	V_{DD}	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}	Operating Voltage		F_{CPU} = 8MHz	1.8	3.0	3.6	V
I_{STB}	Standby Current	3V	No load, System HALT, LVR ON	-	1	-	uA
I_{OH1}	I/O Port Source Current (PA, PC)	3V	V_{OH}=2.7V	-	-1.5	-	mA
I_{OL1}	I/O Port Sink Current (PA, PC)	3V	V_{OL}=0.3V	-	2.5	-	mA
I_{OH2}	I/O Port Source Current (PB4, PY)	3V	V_{OH}=2.7V	-	-6	-	mA
I_{OL2}	I/O Port Sink Current (PB4, PY)	3V	V_{OL}=0.3V	-	6	-	mA
I_{OH3}	I/O Port Source Current (PB4_REM)	3V	V_{OH}=2.7V	-	-1.5	-	mA
I_{OL3}	I/O Port Sink Current (PB4_REM)	3V	V_{OL}=1.5V	-	320	-	mA
R_{PH1}	PA, PC, PY Pull-high R	3V	-	-	300	-	KΩ
R_{PH2}	PA1 Pull-high R	3V	PA1PHS=1	-	10	-	KΩ
V_{IL1}	Input Low Voltage for input port	3V	-	0	-	1	V
V_{IH1}	Input High Voltage for input port	3V	-	2	-	3	V